100 of Figure 1, and items numbered with 2xx numbers in Figures 2a and 2b are meant to correspond to items numbered with 1xx numbers in Figure 1. In a manner corresponding to memory array 100, memory array 200 is comprised of address decoder 220, coupled to memory cell 260 within top half 210 by word line 230, and coupled to memory cell 262 within bottom half 212 by word line 232.

A1 Cont'd

In the paragraph starting on line 3 of page 9:

Regardless of the purpose for having a pair of bit lines connected to each of memory cells 260 and 262, in a manner that corresponds to bit lines 170 and 172 of memory array 100 of Figure 1, in Figure 2a, bit lines 270 and 272 are connected to the inputs of comparator circuit 240, and bit lines 274 and 276 are connected to the inputs of comparator circuit 244. Also corresponding to Figure 1, the outputs of comparator circuits 240 and 244 are connected to latches 242 and 246.

A2

In the paragraph starting on line 1 of page 10:

Furthermore, in an embodiment where memory cells are written to and read from using pairs of bit lines to carry data and its complement and sense amplifiers are used in reading from memory cells, the sense amplifiers could also be configured to serve as the comparators used as the comparator circuits to test the memory cells. This could be accomplished through the use of multiplexers to selectively connect and disconnect different ones of the bit lines as needed to allow the sense amplifiers to perform one or the other of these two functions as depicted by the use of multiplexers 280 and 284 in Figure 2b to selectively couple either one or the other of bit lines 270 or 276 to one input on each of comparators 240 and 244, respectively. Otherwise, in an alternate

A3

A3 cont'd embodiment, the sense amplifiers and the comparators could remain separate components.

In the paragraph starting on line 18 of page 10:

Figure 3 is a block diagram of yet another embodiment of the present invention. Memory array 300 is substantially similar to memory array 200 of Figures 2a and 2b, and items numbered with 3xx numbers in Figure 3 are meant to correspond to items numbered with 2xx numbers in Figures 2a and 2b, with exception of the comparator circuits and their associated latches. In a manner corresponding to memory array 200, memory array 300 is comprised of address decoder 320, coupled to memory cell 360 within top half 310 by word line 330, and coupled to memory cell 362 within bottom half 312 by word line 332. Also in a manner corresponding to memory array 200, memory cell 360 is coupled to bit lines 370 and 374, and memory cell 362 is coupled to bit lines 372 and 376.

A4

In the paragraph starting on line 1 of page 11:

Unlike the embodiments depicted in Figures 2a and 2b, the comparator circuits of Figure 3 are each comprised of a subtracting circuit and a pair of comparators. Bit lines 370 and 372 are connected to the inputs of subtracting circuit 390. Subtracting circuits 390 subtracts the voltage level of one of bit lines 370 from the voltage level of the other of bit lines 372, and outputs a voltage that represents the difference resulting from the subtraction, which could be either a positive or negative voltage output. This output of subtracting circuit 390 is, in turn, connected to one of the two inputs on each of comparators 340 and 341. Correspondingly, bit lines 374 and 376 are connected to the inputs of subtracting circuit 392, and the output of subtracting circuit 392 is connected to one of the two inputs on each of comparators 344 and 345. The other input on

A5

each of comparators 340 and 344 are connected to a high voltage level reference, +vref, and correspondingly, the other input on each of comparators 341 and 345 are connected to a low voltage reference, -vref. The outputs of comparators 340, 341, 344 and 345 are connected to the inputs of latches 342, 343, 346 and 347, respectively.

A5 contd

In the paragraph starting on line 17 of page 11:

Regardless of whether the memory cells of memory array 300 are written to and read from with a pair of bit lines, or each of the two bit lines connected to each cell are meant to be used to perform independent read and write operations, the testing of memory cells 360 and 362 of memory array 300 is carried out in much the same way as was described above for memory cells 260 and 262 in Figures 2a and 2b. However, the configuration of comparator circuits that are each comprised of a subtracting circuit and a pair of comparators as shown in Figure 3 affords greater ability to control the degree to which the voltages on pairs of bit lines that are being compared may differ from each other. More precisely, by adjusting +vref and -vref, comparators 340 and 344 can be biased to allow the voltage levels on bit lines 370 and 372 to differ to a degree that is adjustable before either comparator 340 or 344 outputs a signal indicating a malfunction. If the difference in voltage levels between bit lines 370 and 372 is such that it rises above +vref, then comparator 340 will output a signal indicating so to latch 342, and if the difference in voltages levels between bit lines 370 and 372 is such that it drops below -vref, then comparator 344 will output a signal indicating so to latch 346.

A6